CLAIMS

What I claim is:

1. A waveform generator circuit, comprising:

a triangular and pseudo-sinusoidal waveform generator adapted to accept clock signals and generate triangular waveforms;

an amplitude control current responsively coupled to the triangular and pseudo-sinusoidal waveform generator operable to control the amplitude of the generated triangular waveforms;

a reference voltage circuit responsively coupled to the amplitude control circuit, operable to generate reference voltages for the peak voltages of the triangular waveform;

the triangular and pseudo-sinusoidal waveform generator operable to accept one or a plurality of clock signals;

the triangular and pseudo-sinusoidal waveform generator further operable to generate triangular waveforms from the clock signals,

the triangular and pseudo-sinusoidal waveform generator further operable to rectify the triangular waveforms;

the triangular and pseudo-sinusoidal waveform generator further operable to smooth

the triangular waveforms into pseudo-sinusoidal waveforms.

2. The waveform generator circuit of Claim 1, further comprising the triangular and pseudo-sinusoidal waveform generator being adapted to receive two clock signals with a 90 degree phase difference between them.

3. The waveform generator circuit of Claim 1, further comprising the triangular and pseudo-sinusoidal waveform generator being adapted to output a differential signal.

4. The waveform generator circuit of Claim 1, further comprising the triangular and pseudo-sinusoidal waveform generator being adapted to output a single ended signal.

5. The waveform generator circuit of Claim 1, further comprising being adapted for use in a switching power supply.

6. The waveform generator circuit of Claim 1, wherein the frequency of the output waveforms corresponds to the frequency of the input reference clock.

7. The waveform generator circuit of Claim 1, wherein the common voltage of the triangular waveforms is self-controlled by the circuit using feedback

8. The waveform generator circuit of Claim 1, further comprising being

adapted for use as a differential current mirror.

9. The waveform generator circuit of Claim 1, further comprising:

the reference voltage circuitry generating two reference voltages, one for high side, the other for the low side;

the reference voltage circuitry being operable to supply the two reference voltages to the amplitude control circuitry;

the amplitude control circuitry being operable to generate reference currents to compare to the triangular waveform amplitude;

the amplitude control circuitry being operable to rectify the triangular waveforms and derive the amplitude of the triangular waveforms;

the amplitude circuitry being operable to continuously compare the reference voltage to the amplitude of the triangular waveform to control the supply of the reference currents to the waveform generator; and

the amplitude control circuitry being operable to ensure that the amplitude of the triangular waveform remains constant.

10. The waveform generator circuit of Claim 9, further comprising a voltage-to-current converter responsively coupled to the triangular and pseudo-sinusoidal

waveform generator;

a rectifier within the triangular and pseudo-sinusoidal waveform generator;

and a current comparator responsively coupled to the triangular and pseudo-sinusoidal waveform generator;

the voltage to current converter being operable to convert the waveform voltages and reference voltages into current signals;

the rectifier being operable to add the value of the triangular waveform amplitude to the absolute value of each triangular waveforms to obtain a derived amplitude;

the comparator being operable to compare the derived amplitude to the converted current from the reference voltages;

the comparator having a limited gain;

the comparator being operable to directly control the reference current of the waveform generator.

11. The waveform generator circuit of Claim 1, wherein the triangular and pseudo-sinusoidal waveform generator further comprises:

a triangular waveform generator;

a sinusoidal waveform converter responsively coupled to the triangular waveform

generator;

the sinusoidal waveform generator being adapted to accept a triangular waveform from the triangular waveform generator; and

the triangular waveform having a maximum voltage that will not saturate the output current of the sinusoidal waveform converter.

12. The waveform generator circuit of Claim 11, wherein the sinusoidal waveform generator further has output nodes operable to accept predetermined differential currents.

13. The waveform generator circuit of Claim 1, wherein the triangular and pseudo-sinusoidal waveform generator further comprises:

two triangular waveform differential voltage output nodes "top" and "tom";

two sinusoidal differential current waveform output nodes "sop" and "som";

a first transistor and a second transistor, the sources of the first transistor and second transistor being coupled;

an clock output node coupled to the gate of the second transistor;

the gate of the first transistor being adapted to receive an inverted clock signal for switching purposes;

the gate of the second transistor being adapted to receive a clock signal for switching purposes;

when the clock signal is high and the inverter output is low, the first transistor is on, and the second transistor is off;

the first transistor and second transistor being coupled such that current Ir from a current source flows from the source of the first transistor through the drain of the first transistor;

the source coupled first transistor and second transistor being operable to result in a differential current;

a capacitor coupled to the drain of the second transistor so as to be charged by the differential current, resulting in the voltage at node "top" being increased;

a third transistor and a fourth transistor coupled at their sources;

a fifth transistor and sixth transistor being coupled at their gates and at their sources;

the fifth transistor and sixth transistor being coupled such that the drain current of the fifth transistor and sixth transistor are equal, as both gate-source voltages are equal;

the fifth transistor and sixth transistor being operable to generate common current;

the fifth transistor and sixth transistor being coupled such that when the voltage of the node "top" is increased, the gate-source voltage of the fifth transistor and sixth transistor must increase as the coupled sources of the third transistor and fourth transistor are connected to the gates of the fifth transistor and sixth transistor;

the circuit being operable such that when the voltage at node "tom" is decreased, the drain current of the sixth transistor charges the capacitor;

the circuit further being operable such that when the differential voltage across the capacitor increases, the drain current of the third transistor increases;

the circuit further being operable such that the drain current of the fourth transistor decreases as the voltage across the capacitor increases; and

the drain current of the third transistor and fourth transistor being given by the differential transistor pair V-I characteristic.

14. The waveform generator circuit of Claim 13, further comprising the first, second, third, fourth, fifth and sixth transistors comprising MOSFETs.

15. The waveform generator circuit of Claim 13, further comprising the first, second, third, fourth, fifth and sixth transistors comprising BJTs.

16. The waveform generator circuit of Claim 1, wherein a voltage-to-current converter and a plurality of switches are operable to rectify the triangular waveform, comprising:

a first plurality of transistors configured as switches to transmit currents directly or to exchange currents;

a second plurality of transistors adapted to accept triangular waveform differential voltages at their gates;

a resistor coupled to the second plurality of transistors, the differential input voltage appearing as the voltage across the resistor;

the resistor operable to generate a current proportional to the differential input voltage, the current flowing through the sources and through the drains of the second plurality of transistors; and

a means of swapping the polarity of the output currents at a node such that when the node is high, a set of switches turn on and others turn off.

17. A method of generating a waveform, comprising:

inputting a first clock signal and a second clock signal 90 degrees out of phase with the first clock signal into a waveform generator;

inputting a reference current into the waveform generator;

generating a first triangular waveform and a second triangular waveform that is 90 degrees out of phase from said first triangular waveform from said first clock signal and second clock signal;

inputting said first triangular waveform and second triangular waveform to a first and second voltage-to-current converter;

generating a first and second reference voltage in a reference voltage generator;

inputting the first and second reference voltages to the first and second voltage-to-current generators, respectively;

inputting the first and second currents from the first and second voltage-to-current generators respectively and from the first and second waveform generators to a first and second switch, or plurality thereof, inside of the first and second voltage-to-current converters;

driving the first and second switch or plurality thereof by the clock signal of the other side

controlling the absolute value of the output by summing the output currents from the voltage-to-current generators at a node;

providing the summed current to the input of a current comparator and current bias generator;

comparing the input differential currents at an input node;

increasing a reference current if the current is less than 0 at the input node and hence increasing the amplitude of triangular waveform;

decreasing a reference current if the current is more than a predetermined amount at the input node and hence decreasing the amplitude of triangular waveform; and

rectifying and shaping the triangular waveform to obtain a pseudo-sinusoidal waveform based.

18. The method of generating a waveform of Claim 17, further comprising being operable to serve as a differential current mirror circuit.

19. The method of generating a waveform of Claim 18, further comprising being adapted for use in a switching power supply.

20. The method of generating a waveform of Claim 18, further comprising being adapted for use in a motor driving circuit.